What is claimed is:

1. A memory device comprising:

a first memory array including a plurality of memory cells arranged in columns;

a plurality of first y-drivers, each first y-driver coupled to a corresponding one of a plurality of said columns of memory cells to read contents of memory cells in said column and including a first circuit for testing a level of stored data in the memory cells;

a redundant memory array including a plurality of redundant memory cells arranged in columns;

a plurality of redundant y-drivers, each redundant y-driver coupled to a corresponding one of a plurality of said columns of redundant memory cells to read contents of redundant memory cells in said column and including a second circuit to test a level of stored data in the redundant memory cells; and

a controller to generate a selection signal to enable said redundant y-drivers and to generate a disable signal to disable said first y-drivers in response to a failure of said testing of said level by said first circuit of said corresponding first y-driver.

2. The memory device of claim 1 wherein the first circuit tests a voltage level of the stored data on a bitline coupled to one of said columns of memory cells.

3. The memory device of claim 2 wherein each of the memory cells comprises a transistor having a source, gate, and drain terminals, a first bias voltage is applied to a gate, a second bias voltage is applied to a source of said transistor, and a bias current flowing between the source and drain terminals of said transistor being independent of the data stored in said memory cell.

4. The memory device of claim 2, wherein the first circuit tests a current on a bitline coupled to one of said columns of memory cells, the current being indicative of and dependent on data stored in said memory cell.

5. The memory device of claim 4, wherein each of the memory cells comprises a transistor having a source, gate, and drain terminals, a low voltage is applied to the source, a bias voltage is applied to a gate, and a load is coupled to the drain, the current level is determined from the voltage on said load.

6. The memory device of claim 1 wherein said first and redundant y-drivers each comprise a pattern indicator circuit that comprises a NAND gate to generate an input data pattern indicator in response to input data applied thereto.

7. The memory device of claim 1 wherein each of said first and redundant y-drivers further comprise a pattern indicator circuit to generate an input data pattern indicator in response to received input data.

8. The memory device of claim 7 wherein the input data received substitutes a predetermined data value and said substitution prevented by said disable signal generated by said controller.

9. The memory device of claim 7 wherein the input data pattern indicator inhibits the first y-driver from programming the memory cell in response to a predetermined data value.

10. The memory device of claim 7 further comprising a status latch responsive both to said pattern indicator circuit and to said controller.

11. The memory device of claim 10 wherein said status latch controls inhibiting the first and redundant y-drivers from programming the memory cell in response to a predetermined data value.

12. The memory device of claim 10 further comprising a status flag circuit indicative of the outcome of data read or program operations, said status flag circuit being coupled to said controller.

13. The memory device of claim 12 wherein said status flag circuit is enabled by said status latch and disabled in response to a predetermined data value or disabled in response to said disable signal generated by said controller.

14. The memory device of claim 1 wherein the first circuit includes a comparator having a first input coupled to a reference line for receiving a reference level, having a second input coupled to a data bit line for detecting stored data level, the comparator autozeroing any offset of said comparator before comparison of the reference level and the stored data level.

15. The memory device of claim 1 further comprising a storage circuit for storing addresses of memory cells failing said testing of voltage level of stored data, and wherein said controller generates said selection and disable signals in response to a match between one of the said stored addresses and an applied address signal.

16. The memory device of claim 15 wherein the storage circuit includes a fuse circuit.

17. The memory device of claim 15 further comprising an address sequencer to address the storage circuit to read stored addresses of failing memory cells.

18. The memory device of claim 17 further comprising an address sequencer to read all storage locations of the storage circuit for stored addresses of said failing memory cells.

19. The memory device of claim 15 further comprising an address sequencer to read the locations of the storage circuit having stored addresses of said failing memory cells.

20. The memory device of claim 1 further comprising:

an address sequencer coupled to the controller, the plurality of first y-drivers, and the plurality of redundant y-drivers for generating address signals to address said first y-drivers or redundant y-drivers.

21. The memory device of claim 17 wherein the address sequencer further generates address signals for said defective columns and does not generate address signals for other ones of said columns.

22. The memory device of claim 17 wherein the address sequencer generates said address signals in a predetermined timing relationship with the generation of the selection signal and the disable signal.

23. The memory device of claim 22 wherein the predetermined timing relationship is a real time relationship.

24. The memory device of claim 17 wherein the address sequencer generates the address and the first y-drivers and the redundant y-drivers decode in the address in a time less than the reading of the memory cells.

25. The memory device of claim 17 wherein the address sequencer generates addresses associated with an address of each column of redundant memory cells.

26. The memory device of claim 17 wherein the address sequencer generates addresses associated with an address for each column of redundant memory cells that is enabled and does not generate an address for said columns of redundant memory cells that are not enabled.

27. The memory device of claim 1 wherein the plurality of redundant y-drivers are substantially the same as the first y-drivers and are controlled by an enable signal.

28. The memory device of claim 27 wherein the enable signal is responsive to said controller.

29. The memory device of claim 1 wherein the plurality of memory cells of said first memory array and said redundant memory array are further arranged in a plurality of pages, each column of said plurality of columns being associated with a corresponding page.

30. The memory device of claim 1 wherein said selection and disable signals from said controller are operable upon a group of said redundant and first y-drivers respectively, said group addressed by the smallest address operable by said memory device.

31. The memory device of claim 1 wherein the first memory array is arranged in segments of memory cells, and the controller generates a selection signal for said redundant memory array and generates a disable signal to disable a segment corresponding to a memory cell failing said testing.

32. The memory device of claim 15 wherein the storage circuit comprises a plurality of fuse sets associated with the redundant memory cells, a number of said fuse set is less than the number of columns of redundant memory cells.

33. The memory device of claim 1 further comprising a plurality of fuse sets storing addresses of some memory cells and wherein said fuse set comprises first and second fuse elements, and a latch coupled to the first and second fuse elements for storing the contents of the first and second fuse elements, the first and second fuse elements and the latch being arranged as a differential amplifier.

34. The memory device of claim 33 wherein the memory cells comprise flash transistors, the columns of memory cells arranged in rows and columns, so that a predetermined number of memory cells form a fuse element, and the memory device further comprises at least one dummy row and at least one dummy column of memory cells.

35. The memory device of claim 34 wherein the two cells of each fuse element are disposed on a top portion and a bottom portion, respectively.

36. The memory device of claim 35 wherein one of said at least one dummy rows is disposed on said top portion, another one of said at least one dummy rows is disposed on said bottom portion, one of said at least one dummy column is disposed on a first side portion, and another

one of said at least one dummy column is disposed on a second side portion opposite said first side portion.

37. The memory device of claim 36 wherein others of the dummy rows comprise floating connections.

38. The memory device of claim 35 wherein the column coupled to the bit line does not contact said memory cells except where the memory cells in said column coupled to the bit line are coupled to one of said plurality of fuse sets.

39. The memory device of claim 33 further wherein said fuse set couples to said controller, said controller being responsive to data stored in said fuse set.

40. The memory device of claim 34 wherein the predetermined number of memory cells forming said fuse element is two.

41. The memory device of claim 34 wherein the predetermined number of memory cells forming said fuse element is greater than two.

42. The memory device of claim 34 wherein the predetermined number of memory cells forming said fuse element is three, four or five.

43. The memory device of claim 1 further comprising:

a second memory array including a plurality of second memory cells arranged in columns and for storing an extension and further including an extension y-driver coupled to a corresponding one of a plurality of said columns of second memory cells to read contents of second memory cells in said columns, and including a third circuit for testing a level of stored data in the second memory cells,

wherein said controller generates said selection signal to enable use of said redundant memory arrays and to generate a second disable signal to disable a portion of the second memory array of said data.

44. The memory device of claim 1 wherein data output is multiplexed at the output of the first y-drivers and the redundant y-drivers.

45. The memory device of claim 1 wherein output data is multiplexed at an input/output buffer.

46. The memory device of claim 1 wherein the first and redundant y-drivers comprise an inhibit circuit coupled to a bit line connecting a corresponding one of said plurality of columns of said memory cells to provide an inhibit voltage on said bit line.

47. The memory device of claim 46 wherein the inhibit circuit is a PMOS device.

48. The memory device of claim 46 wherein the inhibit circuit to provide said inhibit voltage on said bit line in response to the first circuit detecting a failure of the level of stored data in the memory cells.

49. The memory device of claim 46 wherein the voltage inhibit circuit provides said inhibit voltage on said bit line in response to a predetermined data value.

50. The memory device of claim 1 wherein the plurality of memory cells in the first memory array are further arranged in a plurality of pages, each page comprising groups of said columns, the controller generating said disable signal to prevent programming of a portion of one page of said first memory array in response to a predetermined data signal and enable another portion of said page to allow programming of said another portion.

51. The memory device of claim 1 further comprising a monitoring circuit coupled to a bit line coupling a column of memory cells.

52. The memory device of claim 1 wherein the memory device and cells are capable of storing N bits of multilevel data per memory cell.

53. The memory device of claim 52 wherein the controller generates the selection signal to enable selected redundant memory cells of one of said columns of said redundant memory array and generates the disable signal to disable corresponding memory cells of one of said columns of said first memory array in response to the failure of said testing of said voltage level, N being an optional number of bits capable of being stored per memory cell when there is no failure of said testing.

54. A memory device comprising:

a first memory array including a plurality of N-bit memory cells that each store 2^N levels and are arranged in columns, and including a plurality of N-bit memory cells that each store less than 2^N levels and are arranged in columns;

a redundant memory array including a plurality of redundant N-bit memory cells that each store 2^N levels and are arranged in columns, and including a plurality of redundant N-bit memory cells that each store less than 2^N levels and are arranged in columns.

55. The memory device of claim 54 wherein a column of said first memory array comprising memory cells storing 2^N levels is replaced by a column of said first memory array comprising memory cells storing less than 2^N levels and a redundant column comprising memory cells storing less than 2^N levels.

56. The memory device of claim 54 wherein a column of the first memory array comprising memory cells storing 2^N levels is replaced by a first redundant column comprising memory cells storing less than 2^N levels and a second redundant column comprising memory cells storing less than 2^N levels.

57. A memory device comprising:

a first memory array including a plurality of memory cells arranged in columns;

a plurality of y-drivers, each y-driver coupled to a corresponding one of said columns of memory cells to read contents of memory cells in said column;

a redundant memory array including a plurality of redundant memory cells;

a plurality of redundant y-drivers, each redundant y-driver coupled to a corresponding one of said columns of redundant memory cells to read contents of redundant memory cells in said column; and

a comparator to detect the contents of selected ones of the plurality of memory cells and having autozeroing of an offset of said comparator.

58. The memory device of claim 57 wherein the memory cells are multilevel memory cells and the comparator compares the contents of said selected ones of the plurality of memory cells to a selected one of a plurality of reference voltages.

59. The memory device of claim 57 further comprising a controller to generate a selection signal to enable said redundant memory array and to generate a disable signal to disable said portion of the first memory array in the event of failing of said testing of said voltage level by said comparator.

60. The memory device of claim 57 wherein the comparator compares a voltage level of the stored data on a bitline coupled to one of said columns of memory cells corresponding to said selected memory cells.

61. The memory device of claim 57 wherein the comparator automatically balances a line for receiving a reference voltage and a line for receiving the stored data prior to application of the reference voltage and the stored data, respectively.

62. A memory device comprising:

a first memory array including a plurality of memory cells arranged in columns;

a plurality of first y-drivers, each first y-driver coupled to a corresponding one of a plurality of said columns of memory cells to read contents of memory cells in said column and including a first circuit for testing a voltage level of stored data in the memory cells and including a bit line monitor circuit coupled to a bit line, said bit line coupled to a corresponding one of a plurality of columns of memory cells, said bit line monitoring circuit providing a signal indicative of the content of one of the corresponding memory cells;

a redundant memory array including a plurality of redundant memory cells;

a plurality of redundant y-drivers, each redundant y-driver coupled to a corresponding one of a plurality of said columns of redundant memory cells to read contents of redundant memory cells in said column; and

a controller to generate a selection signal to enable at least one of said redundant y-drivers and to generate a disable at least one of said first y-drivers in the event of failing of said testing of said voltage level by said first circuit.

63. The memory device of claim 62 wherein said signal from said bit line monitoring circuit is buffered.

64. A method for storing data in a memory system comprising a regular memory cell array, a regular y-driver for determining the data stored in the regular memory cell array, a redundant memory cell array, a redundant y-driver for determining the data stored in the redundant memory cell array, the method comprising:

presetting a predetermined data set in said regular and redundant y-drivers;

determining whether data stored in said regular memory cell array meets a predetermined criteria;

storing data in said regular y-driver and maintaining said predetermined data set in said redundant y-driver in the event the stored data in said regular memory cell array meets said predetermined criteria; and

storing data in said redundant y-driver and maintaining said predetermined data set in said regular y-driver in the event the stored data in said regular memory cell array does not meet said predetermined criteria.

65. The method of claim 64 wherein said storing data in said regular and redundant y-drivers is in pages.

66. The method of claim 64 wherein said memory system further comprising an address decoder for decoding an address indicative of where the data is stored, a controller for generating a selection signal enabling said redundant y-drivers and generating a disable signal disabling said

regular y-drivers in response to a failure of said determining the data stored in the regular memory cell array, an address fuse for storing failing addresses, the determining step comprising:

comparing the decoded address to a failing address stored in the address fuse; and

disabling said regular y-drivers and enabling said redundant y-drivers in the event the stored data in said regular memory cell array does not meet said predetermined criteria.

67. The method of claim 66 wherein said storing data in enabled ones of said regular and redundant y-drivers replaces said predetermined data set with data in.

68. The method of claim 67 wherein if said predetermined data set has been maintained in ones of said regular and redundant y-drivers, said predetermined data set disables programming the corresponding memory cell array.

69. The method of claim 64 wherein said storing data in comprises storing N bits of data per cell where N>1.

70. The method of claim 64 wherein said storing data in comprises storing N bits of data per cell where N>2.

71. A method for writing data in a memory system comprising a regular memory cell array, a regular y-driver for determining the data stored in the regular memory cell array, a redundant memory cell array, a redundant y-driver for determining the data stored in the redundant memory cell array, the method comprising:

determining whether data stored in said regular memory cell array meets a predetermined criteria;

verifying data stored in said regular memory cell array and in said redundant memory cell array;

setting a compare-OR flag in the event said verifying meets a criteria;

rewriting the data in said regular y-driver in the event said compare-OR flat is not set and in the event the stored data in said regular memory cell array meets said predetermined criteria, and repeating said verifying until the maximum count is reached;

rewriting the data in said redundant y-driver in the event said compare-OR flag is not set and in the event the stored data in said regular memory cell array does not meet said predetermined criteria, and repeating said verifying until a maximum count is reached;

verifying the margin stored in said regular memory cell array and in said redundant memory cell array;

setting the compare-OR flag in the event said verifying of the margin meets a criteria; and

setting error flag in the event said verifying of the margin does not meet said criteria.

72. The method of claim 71 wherein said writing of data said regular and redundant y-drivers is in pages.

73. The method of claim 71 wherein said memory system further comprising an address decoder for decoding an address indicative of where the data is stored, a controller for generating a selection signal enabling said redundant y-drivers and generating a disable signal disabling said regular y-drivers in response to a failure of said determining the data stored in the regular memory cell array, an address fuse for storing failing addresses, the determining step comprising:

comparing the decoded address to a failing address stored in the address fuse; and

disabling said regular y-drivers and enabling said redundant y-drivers in the event the stored data in said regular memory cell array does not meet said predetermined criteria.

74. The method of claim 73 wherein said setting the compare-OR flag is responsive to only enabled ones of said regular and redundant y-drivers.

75. The method of claim 73 wherein said setting the error flag is responsive to only enabled ones of said regular and redundant y-drivers.

76. The method of claim 71 wherein said writing comprises writing N bits of data per cell where N>1.

77. The method of claim 71 wherein said writing data in comprises writing N bits of data per cell where N>2.

78. A method for erasing data in a memory system comprising a regular memory cell array, a regular y-driver for determining the data stored in the regular memory cell array, a redundant memory cell array, a redundant y-driver for determining the data stored in the redundant memory cell array, the method comprising:

applying an erase signal to the regular and redundant memory cell arrays;

determining whether data stored in said regular memory cell array meets a predetermined criteria;

verifying the erase margin stored in said regular memory cell array and in said redundant cell array;

setting a compare-OR flag in the event said verifying meets a criteria;

incrementing addresses of cells of the regular memory cell array and said redundant memory cell array;

repeating said applying, verifying, setting and incrementing in the event the compare-OR flag is set; and

setting an error flag in the event the compare-OR flag is not set.

79. The method of claim 78 further comprising erasing data in pages.

80. The method of claim 78 wherein the setting an error flag in the event the compare-OR flag is not set includes repeating said applying, verifying, setting, and incrementing in the event the compare-OR flag is not set a predetermined number of times.

81. The method of claim 78 wherein said erase signal has a variable erase time.

82. The method of claim 78 wherein said erase signal has a variable erase level.

83. The method of claim 82 wherein said erase signal has a variable erase time.

84. The method of claim 78 wherein said memory system further comprising an address decoder for decoding an address indicative where the data is stored, a controller for generating a selection signal enabling said redundant y-drivers and generating a disable signal disabling said regular y-drivers in response to a failure of said determining the data stored in the regular memory array, an address fuse for storing failing addresses, the determining step comprising:

comparing the decoded address to a failing address stored in the address fuse; and

disabling said regular y-drivers and enabling said redundant y-drivers in the event the stored data in said regular memory cell array does not meet said predetermined criteria.

85. The method of claim 84 wherein said setting the compare-OR flag is responsive to only enabled ones of said regular and redundant y-drivers.

86. The method of claim 84 wherein said setting the error flag is responsive to only enabled ones of said regular and redundant y-drivers.

87. The method of claim 78 wherein said writing comprises writing N bits of data per cell where N>1.

88. The method of claim 78 wherein said writing data in comprises writing N bits of data per cell where N>2.

89. A method for reading data in a memory system comprising a regular memory cell array, a regular y-driver for determining the data stored in the regular memory cell array, a redundant memory cell array, a redundant y-driver for determining the data stored in the redundant memory cell array, the method comprising:

determining whether data storing in said regular memory cell array meets a predetermined criteria;

reading data stored in said regular memory cell array and in said redundant memory cell array;

shifting out data stored in said regular memory cell array in the event the stored data in said regular memory cell array meets said predetermined criteria; and

shifting out data stored in said redundant memory cell array in the event the stored data in said regular memory cell array does not meet said predetermined criteria.

90. The method of claim 89 wherein said reading of data from said regular and redundant y-drivers is in pages.

91. The method of claim 89 further comprising between the reading and shifting steps:

verifying the restore margin of data stored in said regular memory cell array and said redundant memory cell array; and

setting a compare-OR flag in the event said verifying meets a criteria.

92. The method of claim 91 wherein said memory system further comprising an address decoder for decoding an address indicative of where the data is stored, a controller for generating a selection signal enabling said redundant y-drivers and generating a disable signal disabling said regular y-drivers in response to a failure of said determining the data stored in the regular memory array, an address fuse for storing failing addresses, the determining step comprising:

comparing the decoded address to a failing address stored in the address fuse; and

disabling said regular y-drivers and enabling said redundant y-drivers in the event the stored data in said regular memory cell array does not meet said predetermined criteria.

93. The method of claim 92 wherein said setting the compare-OR flag is responsive to only enabled ones of said regular and redundant y-drivers.

94. The method of claim 89 wherein said reading comprises reading N bits of data per cell where N>1.

95. The method of claim 89 wherein said reading data in comprises reading N bits of data per cell where N>2.

96. The method of claim 89 wherein said reading comprises:

sensing a voltage value stored in the memory cell;

for each bit of N-bit data value where N is the number of bits stored in a cell,

determining a comparison value based on the bit to be determined and any previously determined bits,

comparing the value sensed from the memory cell against the comparison value, and

indicating the bit as a one or a zero based on a result of the comparing.

97. The method of claim 91 wherein said verifying the restore margin comprises:

comparing voltage of a data cell in the regular or redundant memory arrays to at least one first reference voltage minus a predetermined voltage and to at least one second reference voltage plus a predetermined voltage, said first and second reference voltages corresponding to a range of multilevel data stored in a cell.